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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,891	12/19/2001	Gee Sung Chae	8733.495.00	8845

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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,891	CHAE, GEE SUNG	
	Examiner	Art Unit	
	Thoi V.Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 15, 2004 has been entered.

Accordingly, claim 28 was amended, and claims 1-17 were cancelled. Currently, claims 18-41 are pending in this application.

Allowable Subject Matter

2. The indicated allowability of claims 18-27 is withdrawn in view of the newly discovered reference(s) to USPN 6,529,251 B2 of Hibino et al. and USPN 5,995,187 of Wakagi et al.. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hibino et al. (USPN 6,529,251 B2) in view of Wakagi et al. (USPN 5,995,187).

Re claims 18 and 28, as shown in Fig. 1, Hibino et al. discloses a liquid crystal display (LCD) as well as a method of fabricating the same comprising:

a gate electrode 12 formed on a substrate 11;

a gate insulating film 16 formed on an entire surface of the substrate;

a semiconductor layer 17 and an ohmic contact layer 18 formed on the gate insulating film;

a buffer layer 20 formed on the ohmic contact layer;

a pixel electrode 26 formed on the buffer layer;

source and drain electrodes 21 connected with the pixel electrode on the buffer layer; and

a passivation layer 24 formed on a surface of the substrate.

Hibino et al. discloses all aspects of claims 18 and 28 as shown above except for forming a common electrode on the passivation layer. As shown in Fig. 1, Wakagi et al. discloses an in-plane switching mode liquid crystal display (LCD) device comprising a pixel electrode 11 and a common electrode 12 formed on an insulation layer 9 for applying electric fields parallel to substrates so as to reduce losses in the driving voltage applied to the liquid crystal (col. 1, line 66 through col. 2, line 22). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Hibino et al. with the teaching of Wakagi et al. by forming a common electrode on the passivation layer to reduce losses in the driving voltage applied to the liquid crystal (col. 1, lines 66-67).

Re claims 27 and 34, Hibino et al. does not disclose a common electrode formed of indium tin oxide. Wakagi et al. also suggests that the common electrode includes indium tin oxide for reducing the contact resistance and being able to transmit a visible light (col. 3, lines 54-56 and col. 4, lines 15-23). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Hibino et al. with the teaching of Wakagi et al. by forming a common electrode including indium tin oxide for reducing the contact resistance and being able to transmit a visible light (col. 3, lines 54-56 and col. 4, lines 15-23).

Re claims 19, 20 and 29, Hibino et al. discloses that the gate electrode 12 includes aluminum (Al) (col. 5, lines 54-56), which is a low resistance material.

Re claims 21, 22 and 30, Hibino et al. discloses that the buffer layer 20 includes titanium (Ti) (col. 5, lines 59-62).

Re claims 23, 24 and 31, Hibino et al. discloses that the source and drain electrodes 21 include aluminum (Al) (col. 5, lines 59-62).

Re claims 2, 26 and 32, Hibino et al. discloses that the pixel electrode includes indium tin oxide (col. 8, lines 61-62).

Re claim 33, Hibino et al. discloses that the drain electrode 21 is electrically connected with the pixel electrode (Fig. 1).

Re claim 35, Hibino et al. discloses that the gate electrode 12 is deposited by a sputtering process (col. 6, lines 50-56),

Re claim 36, Hibino et al. discloses that the gate electrode 12 is patterned using photolithography (col. 6, lines 60-63),

Re claims 37 and 38, Hibino et al. discloses that the semiconductor layer 17, the ohmic contact layer 18, and the buffer layer 20 are formed on the gate insulating film 16 by a plasma enhanced chemical vapor deposition (PECVD) process, wherein the semiconductor layer, the ohmic contact layer, and the buffer layer are patterned (col. 7, lines 15-60),

Re claims 39 and 40, Hibino et al. discloses that the pixel electrode is formed by a sputtering process, wherein the pixel electrode is patterned (col. 8, lines 61-67).

Finally, re claim 41, Hibino et al. discloses that the passivation layer 24 is formed by a deposition process (col. 7, lines 63-67).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

05/22/2004

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